Abstract of the Disclosure

An apparatus and method for detecting errors in received data and transferring only error-free data in data communications are provided. In the cyclic redundancy check (CRC) verification apparatus and method having a constant delay, irrespective of the length of a received data frame, input and output processing delay of received data is made to be constant. The CRC verification apparatus having constant delay comprises an input control unit which stores the start address of an input data frame in a memory storing the input data frame, and stores a CRC verification result in the start address location; and an output control unit which after a predetermined constant time passes from the start address, reads an input data frame and if the CRC verification result is normal, output the read data frame. The apparatus and method make the time taken for receiving a data frame, constant irrespective of the received data frame, while CRC verification is performed.